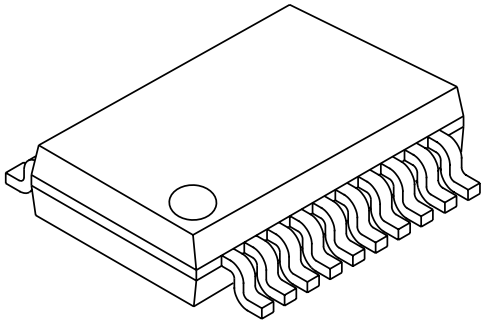
DATA SHEET



BZA109TS
9-fold ESD Transient Suppressor

Preliminary specification
File under Discrete Semiconductors, SC01

1997 Sep 08

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9-fold ESD Transient Suppressor BZA109TS

FEATURES

- ESD rating > 8 kV, according to IEC1000-4-2
- SOT339 surface mount package
- Common anode configuration
- Non-clamping range 0 - 6.8 V, negative clamping range <0.5 V, positive clamping range >6.8 V.

DESCRIPTION

Monolithic silicon zener diode in a SOT339-1 package (SO20) for 9 bit wide undershoot/overshoot clamping, combined with fast ESD transient suppression.

APPLICATIONS

- Computer and peripherals
- Audio and video equipment
- Communication systems
- Medical equipment.

PINNING SOT339-1

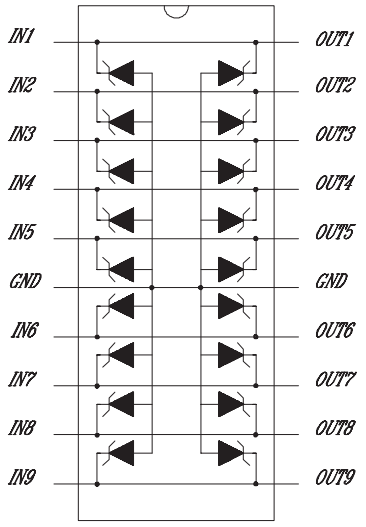


Fig.1 Symbol and pinning.

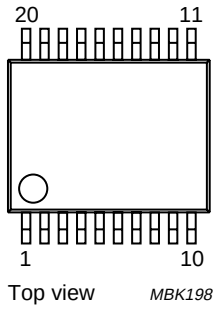


Fig.2 Simplified outline.

LIMITING VALUES (per diode)

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_Z	reverse current	DC; T_{amb} = 25 °C	–	20	mA
I_F	forward current	DC; T_{amb} = 25 °C	–	100	mA
I_{FT}	feed-through current	DC; T_{amb} = 25 °C; note 1	–	100	mA
I_{FSM}	peak forward current	t_p = 1 ms; square wave	–	4.5	A
I_{ZSM}	peak reverse current	t_p = 1 ms; square wave		2.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 2	–	0.95	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 2	135	K/W

Note to the Limiting values and Thermal characteristics

1. Current is flowing from input to corresponding output.
2. One or more diodes loaded.

ELECTRICAL CHARACTERISTICS (per diode)

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_Z	reverse voltage	I_Z = 250 μA	6.4	6.8	7.2	V
V_F	forward voltage	I_F = 100 mA	–	–	1.1	V
V_{ZSM}	reverse surge voltage	t_p = 1 ms; I_{ZSM} = 2.5 A	–	–	10	V
I_H	input high current	V_{IN} = 5.25 V	–	–	0.5	μA
R_Z	zener impedance	I_Z = 250 μA	–	–	100	Ω
S_Z	temperature coefficient of V_Z		–	3	–	mV/K
C_D	input diode capacitance	f = 1 MHz; V_R = 0	–	–	200	pF
		f = 1 MHz; V_R = 5.25 V	–	–	100	pF

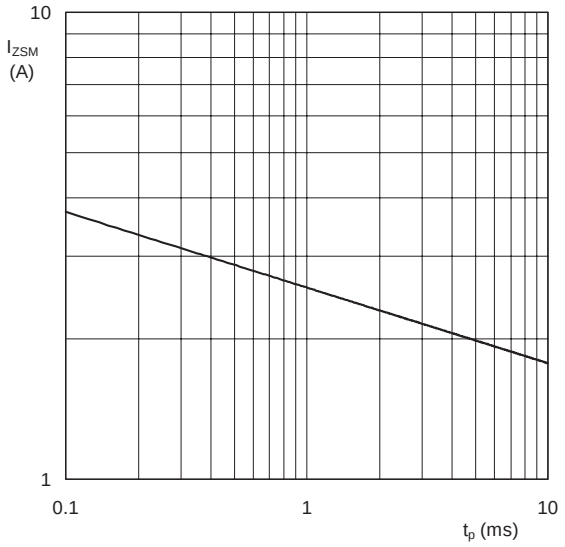
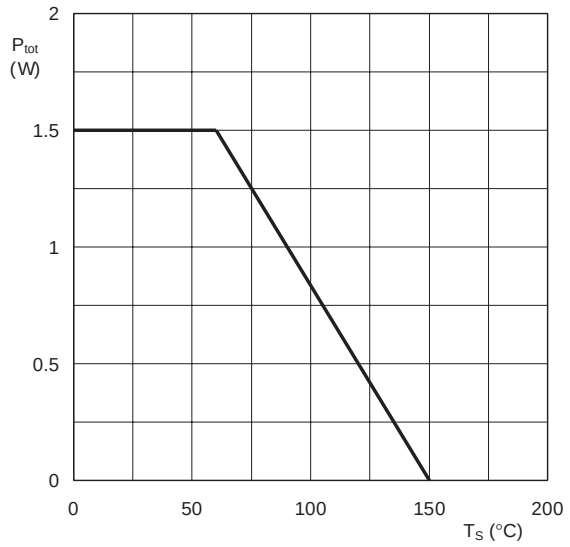
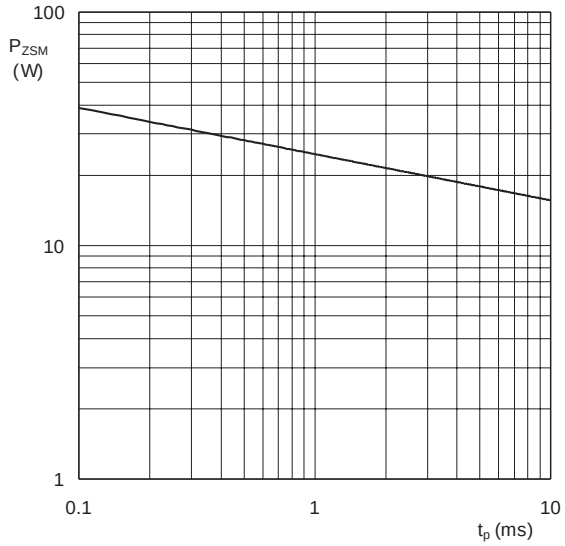


Fig.3 Maximum non-repetitive peak reverse current as a function of the pulse time.



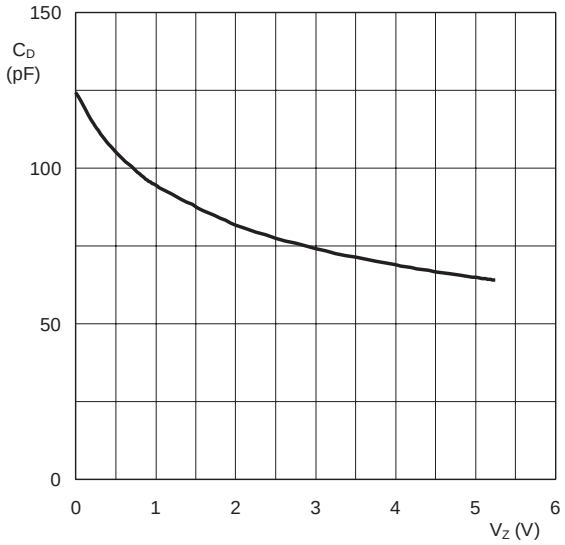
All diodes loaded.

Fig.4 Power derating curve.



$P_{ZSM} = V_{ZSM} \times I_{ZSM}$;
V_{ZSM} is the non-repetitive peak reverse voltage at I_{ZSM}.

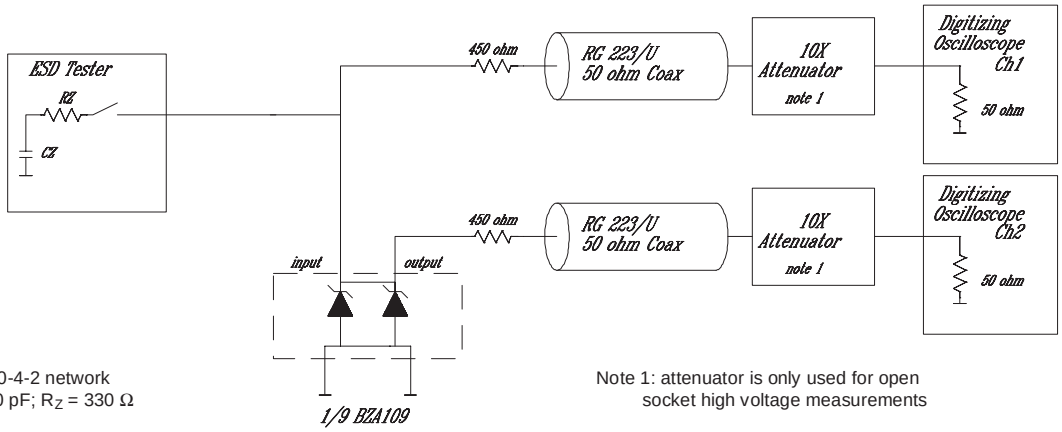
Fig.5 Maximum non-repetitive peak reverse power dissipation as a function of the pulse duration (square pulse).



T_j = 25 °C; f = 1 MHz.

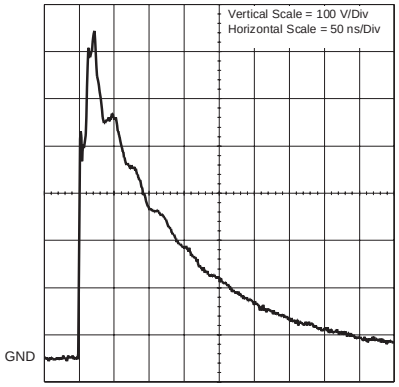
Fig.6 Diode capacitance as a function of the working voltage; typical values.

GRAPHICAL DATA

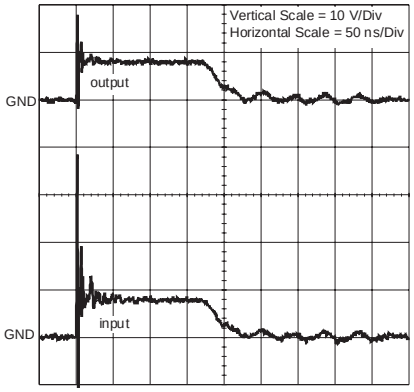


IEC 1000-4-2 network
C_Z = 150 pF; R_Z = 330 Ω

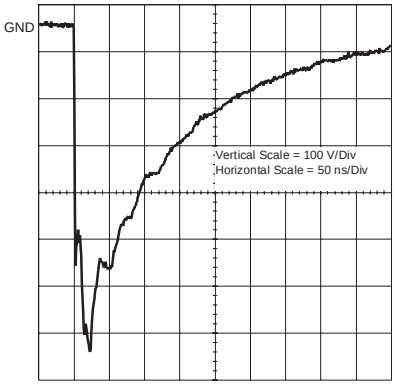
Note 1: attenuator is only used for open socket high voltage measurements



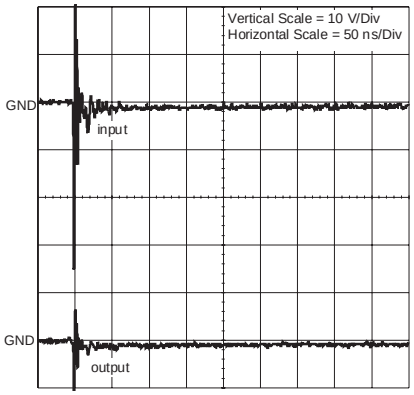
Unclamped +1 kV ESD Voltage Waveform
(IEC1000-4-2 network)



Clamped +1 kV ESD Voltage Waveform
(IEC1000-4-2 network)



Unclamped -1 kV ESD Voltage Waveform
(IEC1000-4-2 network)



Clamped -1 kV ESD Voltage Waveform
(IEC1000-4-2 network)

Fig.7 ESD clamping test set-up and waveforms.

TYPICAL COMMON ANODE APPLICATION

A nine-fold transient suppressor in a SOT339 package gives the possibility to protect nine separate lines using only one package. Two simplified examples are illustrated below.

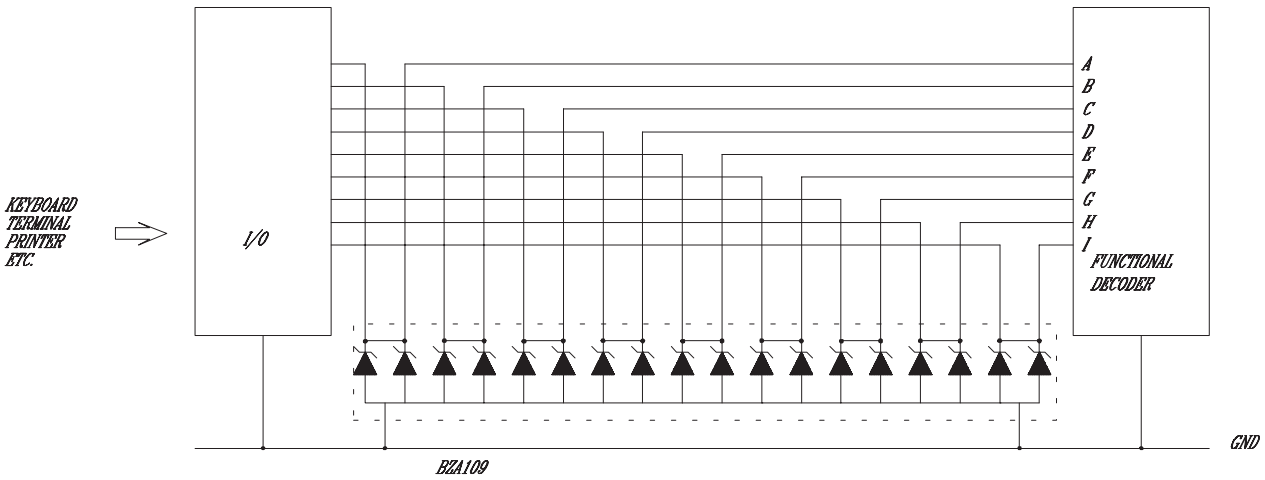


Fig.8 Computer interface protection.

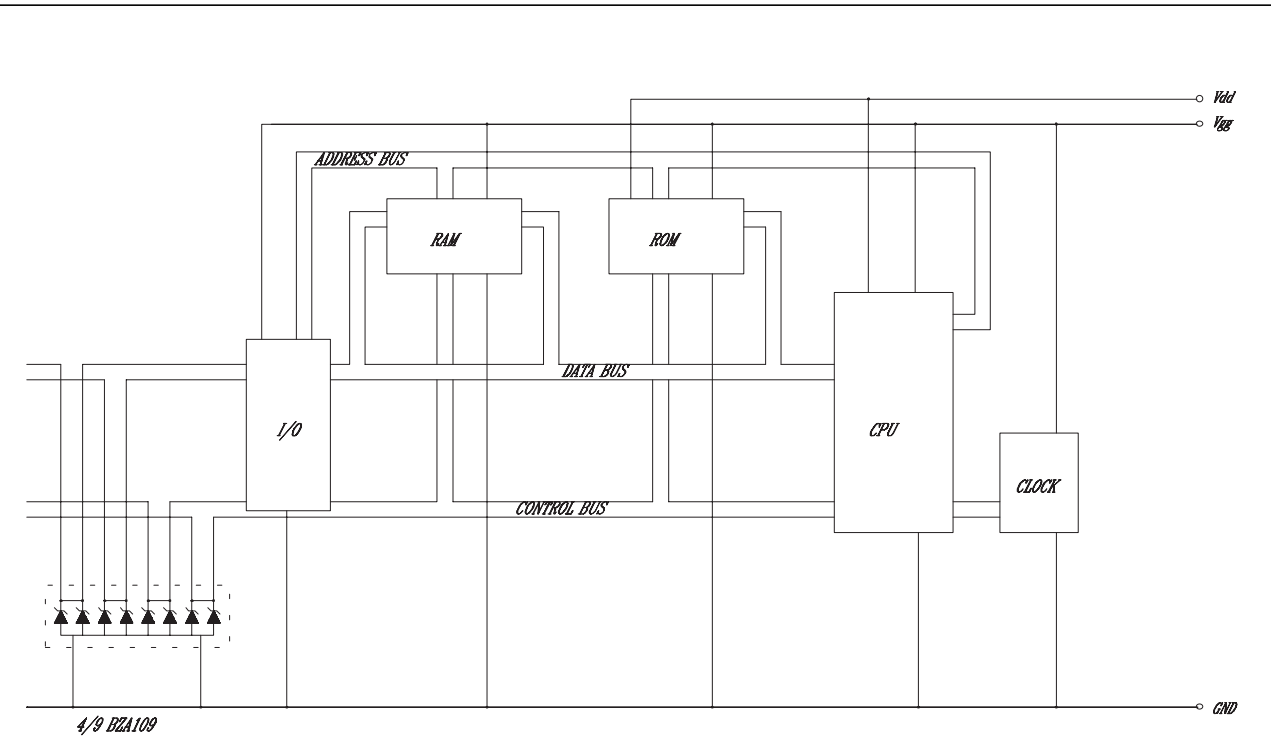


Fig.9 Microprocessor protection.

DEVICE PLACEMENT AND PRINTED-CIRCUIT BOARD LAYOUT

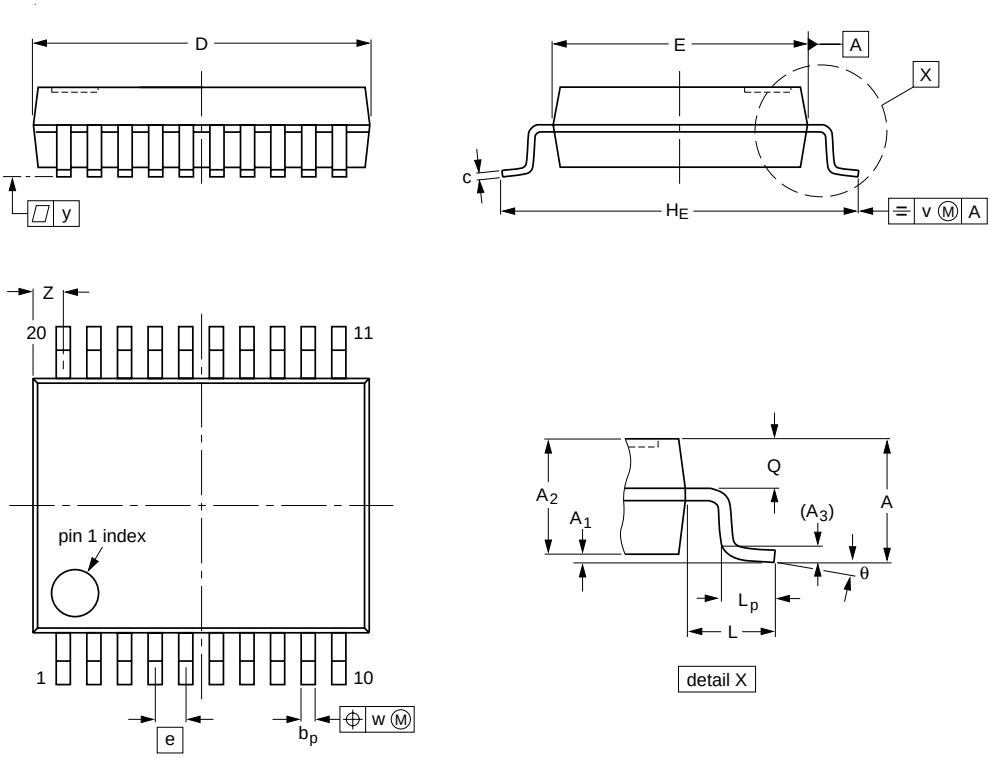
Circuit board layout is of extreme importance in the suppression of transients. The clamping voltage of the BZA109TS is determined by the peak transient current and the rate of rise of that current (di/dt). Since parasitic inductances can further add to the clamping voltage (V = L di/dt) the printed-circuit board layout should use minimal series conductor lengths. This includes the lead length of the suppression element.

In addition to minimizing conductor length the following printed-circuit board layout guidelines are recommended:

1. Place the suppression element in the area of the input terminals or connectors.
2. Reduce parallel signal paths.
3. Avoid running protection conductors in parallel with unprotected conductors.
4. Minimize all printed-circuit board loop areas including power and ground loops.
5. Minimize the length of the transient return path to ground.
6. Avoid using shared transient return paths to a common ground point.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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